REQUEST FOR PROPOSAL (RFP)

for

FABRICATION AND DELIVERY OF SAC DESIGNED RFIC

SPACE APPLICATIONS CENTRE

INDIAN SPACE RESEARCH ORGANISATION

GOVERNMENT OF INDIA

AHMEDABAD-380015

INDIA

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CONTENTS

1.0 **Introduction:** 3
2.0 **Scope of Work:** 3
3.0 **Delivery Schedule:** 5
4.0 **Deliverables:** 6
5.0 **Packaging, Storage and Transportation:** 6
6.0 **Proprietary Rights:** 7
7.0 **Warranty:** 7
8.0 **General Guidelines:** 7
9.0 **Payment Terms :** 8
10.0 **Evaluation Criteria:** 8

1.0 Introduction:

Space Applications Centre (SAC), Indian Space Research Organisation (ISRO), is involved in realization of remote sensing satellites for earth observations, meteorological applications, oceanography, and planetary applications. With current need of miniaturization of entire system electronics, miniaturization of RF frequency synthesizer is to be carried out.

SAC has initiated in-house development of radio frequency integrated circuits (RFIC) for development of Phase Locked Loop and other RF circuits required for the development of RF synthesizer. SAC proposes to use 180nm Silicon Germanium (SiGe): BiCMOS process with support of both 1.8V and 3.3V FETs for design of RF circuits.

2.0 Scope of Work:

2.1 SAC/ISRO Responsibility:

2.1.1 SAC will design RF frequency synthesizer consists of RF sub-circuits i.e. Phase-frequency detector (PFD), oscillator, counters, filter, frequency divider, reference bandgap, amplifier, LNA, multiplier, mixers, charge pump, etc. in size upto 5mmx5mm.
2.1.2 SAC will provide GDSII data compatible to 180nm Silicon Germanium (SiGe): BiCMOS process. Specifications of the process are listed in Table I.

Process Specifications:

Table-I Process Specification

Sr. No.	Process parameter	Specification	Vendor's Compliance
1.	Transistor technology	0.18um SiGe : BiCMOS	
2.	Cut-off Frequency (f_T)	> 60 GHz	
3.	Device Types (for RF and digital circuits)	Heterojunction Bipolar Transistors (emitter widths up to 0.15µm) NMOSFETs & PMOSFETs (channel lengths up to 0.18µm) MOS Varactor, diodes.	
4.	Operating Voltages (MOSFETs & HBTs)	≤ 3.3V	
5	Passives	MIM Capacitors Poly resistors and metal resistors Spiral inductors	
6	NF_{min} and Associated Gain for an HBT	NF_{min} : ≤ 0.7dB typical @2.5GHz; ≤ 1.5dB typical @ 10GHz Gain: >12dB typical @2.5 GHz; >10dB typical @ 10GHz	
7	Isolation	Deep trench, Deep NWell	
8	Number of metal levels	> 3	

Process Design Kit:

The process design kit should have the following:

Sr. No.	RFP Requirements	Vendor's Compliance
1	Linear & Non-Linear scalable RF models for active devices including statistical and noise models.	
2	Scalable RF models and statistical models for passives.	
3	Scalable RF and statistical models for MOS varactors and diodes.	
4	Models of via holes for interconnection between various metal layers	
5	RF/DC Pads	
6	Substrate and metal definition for EM simulation	
7	ESD design library and support for the models required for the design simulation with ESD pads.	
8	Quantus, Calibre, Assura and PVS compatible file for DRC, LVS, PEX and dummy fill files.	

2.2 Foundry/Vendor Responsibility:

Sr. No.	RFP Requirements	Vendor's Compliance
2.2.1	Quote for the above process in Multi Project Wafer (MPW) run for die sized mentioned in Table-II and process specifications mentioned in table I.	
2.2.2	Provide latest updated Process Design Kit (PDK)	
2.2.3	Provide MPW schedule of foundry from initialization of contract to delivery of RFIC.	
2.2.4	Fabricate as per SAC design using 180nm Silicon Germanium (SiGe): BiCMOS process. Vendor must fabricate at least 50 visually good dies with PCM cleared data for each sub-diced circuit. 20 packaged devices shall be delivered to SAC.	
2.2.5	Package procurement and Packaging of 20 dies in standard QFN package not more than 64 pins, and in not more than 9mm X 9mm package size.	

Table – II shows the responsibility of SAC and the foundry for each run:

Table-II

Sr No.	Activity	Activity by SAC	Activity by foundry
1.	Supply of RFIC design libraries (PDKs) compatible to ADS and Cadence including statistical data.		✓
2.	Design of RFIC [up to 5mmx5mm] area	✓	
3.	Final layout in GDS II	✓	
4.	DRC check	✓	✓
5.	Fabrication of RFIC in MPW mode		✓
6.	Wafer dicing, picking and placing visually good dies in gel packs (total:50 numbers of each sub diced circuit)		✓
7.	20 numbers of packaged devices (standard QFN package not more than 64 pin, and in not more than 9mm X 9mm package size).		✓
8.	Delivery of RFIC as per details in Table-III.		✓

3.0 Delivery Schedule:

Time schedule for the execution of contract shall be as per Table-III for each RFIC MPW run.

Table - III

Sr No.	Activity	Activity duration	Vendor's Compliance
1.	Foundry DRC cleared GDS-II data for fabrication	T_0	
2.	Delivery of 50 numbers of visually good dies for each sub-diced circuit.	$T_1 = T_0 + 8$ months	
3.	Delivery of 20 number of packaged devices (out of total visually good dies)	$T_3 = T_2 + 5$ months	

NOTE:

Sr. No.	RFP Requirements	Vendor's Compliance
1.	SAC will load GDS-II of first MPW run typically within 10 months of PO placement.	
2.	T_2 will be free issue material of 20 number of visually good dies. T_2 will be within 30 days of T_1.	
3.	GDS-II of second and third MPW run will be loaded within contract duration and the schedule for development will be as per Table III.	
4.	For LD calculation, T_0 and T_2 for each run shall be considered as reference.	
	Please refer Sr. No 5 of Clause 8: General Guidelines for further details.	

4.0 Deliverables:

Below table mentions the list of deliverables for each RFIC MPW run:

Sr. No.	RFP Requirements	Vendor's Compliance
1.	50 dies of each sub-diced circuit for each MPW run.	
2.	20 numbers of packaged device for each MPW run as per package and pin configuration mentioned in Table II.	
3.	Data pack consisting of: standard PCM data including parameters given below. Threshold voltages, Breakdown voltages, Saturation currents, Contact resistance for vias, Sheet resistance for metal layers and resistors.	

5.0 Packaging, Storage and Transportation:

Sr. No.	RFP Requirements	Vendor's Compliance
1.	Standard Quad flat no lead (QFN) package compatible with die size and pin count as provided by SAC.	
2.	Vendor must provide the high-resolution photograph of wire bonds and pads taken before closing the lid of packages and an X-ray of packaged devices.	
3.	Fabricated devices shall be packaged in ESD safe gel packs, to ensure that they are isolated from electrical, mechanical and environmental damage.	
4.	The packages for the devices shall be purged with nitrogen or evacuated, so that the devices are not exposed to external environment.	
5.	The packaging shall be so as to prevent effect of mechanical shocks, humidity and dust.	
6.	In addition to other mandatory shipping marking, it shall be mentioned on the shipping package that contents are fragile, static sensitive, to be opened under clean environment with ESD protection only, store in a cool and dry place.	
7.	It is to be noted that "pink poly-foam" shall not be used for packing of the individual devices, as it has a corrosive effect on gold plating of the device body and leads.	

6.0 Proprietary Rights:

Sr. No.	RFP Requirements	Vendor's Compliance
1.	The RFIC designs will be properties of SAC and will not be reproduced anywhere without permission of SAC.	

7.0 Warranty:

Sr. No.	RFP Requirements	Vendor's Compliance
1.	The supplier hereby warrants that the products to be supplied under this order are visually good dies in all respects including material, workmanship, performance and shall continue to so during warranty period specified below.	
2.	For a period of 1 year from the date of delivery of products, any defects related to fabrication discovered therein or any defects there in found to have developed under proper use arising from faulty materials. The supplier shall remedy such defects at his own cost, whenever notified by the purchaser in writing.	

8.0 General Guidelines:

Sr. No.	RFP Requirements	Vendor's Compliance
1.	The vendor is requested to acknowledge the receipt of this RFP and his willingness/ability to respond and quote against this RFP.	
2.	The vendor must be the authorized agency/partner of the foundry and letter of authorization/partnership should be submitted along with the quotation.	
3.	The vendor must ensure that his quotation along with all the details reaches SAC before the due date.	
4.	The vendor is requested to examine the RFP thoroughly and offer compliance/non-compliance point by point. Vendor should clearly specify the offered process technology name.	
5.	Contract Validity is 6 years (SAC shall load all GDS within 6 years of PO placement). However, if GDS is not loaded within stipulated timeframe, the contract could be extended further up to 2 years with the same terms and conditions, based on mutual agreement.	
6.	The commercial quotation should include details shown in Table – IV. 1 lot refers to 50 numbers	

	of dies from each sub-diced circuit. MPW costing should include at least 4 die cuts.	
7.	Collection of dies from SAC for packaging should be vendor’s responsibility. BG would be INR 10 lacs against Sr no. 2, 4, and 6 and needs to be submitted based on execution of the same and is valid for the entire contract period.	
8.	Vendor must provide all technical data necessary, in case this is not already in public domain the vendor is requested to obtain necessary clearance.	
9.	If there is rejection of dies is due to process related problem, foundry must re-fabricate SAC design without additional cost.	
11.	Foundry need to identify and share contact/mail-id details of one focal person to interact for design kit, design manual & process review.	
12.	SAC reserves the right to execute the number of MPW runs and packaging as per requirement.	
13.	Typical design cycle is 10 months for each run.	

Table - IV

Sr. No.	Item	Cost
1.	Visually known good dies of first MPW run (1 lot)	
2.	Packaged devices of first MPW run (Qty-20)	
3.	Visually known good dies of second MPW run (1 lot)	
4.	Packaged devices of second MPW run (Qty-20)	
5.	Visually known good dies of third MPW run (1 lot)	
6.	Packaged devices of third MPW run (Qty-20)	
Total		

9.0 Payment Terms :

The payment for each MPW run will be on pro-rata basis against delivery for each run.

1. Delivery of visually known good dies.
2. Delivery of packaged devices against submission of BG (Refer to Sr.No. 7 of Clause 8: General Guidelines).

10.0 Evaluation Criteria:

Criteria for L1 evaluation will be based on total cost of Sr. No. 1 to 6 in table IV.

Formula for total cost calculation for deciding L1: Sr. No. (1 + 2+ 3+ 4+ 5+ 6).