Annexure-1

A

REQUEST FOR PROPOSAL (RFP)

For

Fabrication and delivery of Generic RADAR Waveform Synthesis ASIC using 65nm/55nm CMOS Process

SPACE APPLICATIONS CENTRE

INDIAN SPACE RESEARCH ORGANISATION

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INTRODUCTION:

Space Applications Centre (SAC), Indian Space Research Organization (ISRO), is involved in realization of remote sensing satellites for earth observations, meteorological applications, and planetary applications. Microwave Remote Sensing Area has initiated development of Application specific integrated circuits (ASICs) to achieve high computation with low power, low size and volume requirements. As a step towards miniaturization of electronics, fabrication of SAC designed Generic RADAR Waveform Synthesis (GRWS) ASIC consisting of Dual channel DAC (Digital to Analog Convertor) and DDCS (Direct Digital Chirp Synthesis) integrated on a single chip, is proposed using 65nm/55nm CMOS process node. The ASIC will be fabricated in latest MPW run.

<table>
<tr><th>Sr. No.</th><th>Description</th><th>Compliance</th><th>Remarks</th></tr>
<tr><td>1</td><td>Specifications
<table>
<tr><th>Sr. No.</th><th>Parameter</th><th>Specifications</th></tr>
<tr><td>1.</td><td>Die Area</td><td>Minimum 25 sq.mm.</td></tr>
<tr><td>2.</td><td>Process technology node</td><td>CMOS-65nm/55nm</td></tr>
<tr><td>3.</td><td>Analog Core Voltage</td><td>3.3V</td></tr>
<tr><td>4.</td><td>Digital Core Voltage</td><td>Less than 1.8V</td></tr>
<tr><td>5.</td><td>IO pad Voltage</td><td>3.3V,2.5V</td></tr>
<tr><td>6.</td><td>Package</td><td>256-pin QFP</td></tr>
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<tr><td>2</td><td>Foundry/Vendor Responsibility

1) Fabricate ASIC as per SAC design using 65nm/55nm CMOS process. Vendor has to fabricate at least 50 Process Control Monitor (PCM) cleared visually good dies, so that 40 dies and 10 packaged devices shall be delivered to SAC.
2) Vendor has to carry out packaging of fabricated dies in compatible QFP package.
3) Provide MPW (Multi Project Wafer) schedule of foundry.
4) PDK related support should be provided.
5) The vendor must provide comprehensive PDK related training for designing in their process (Mode of training: Online, Duration: tentatively 2 days).</td><td></td><td></td></tr>
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Table -1 shows the responsibilities of SAC and the foundry/vendor for GRWS ASIC.

Table -1

Sr. No.	Activity	Activity Carried by SAC	Activity Carried by Foundry/Vendor
1.	Supply libraries (PDKs) (Note-1)		✓
2.	Design of GRWS ASIC	✓	
3.	DRC Check	✓	
4.	Final layout in GDS II	✓	
5.	DRC Check at Chip Level	✓	✓
6.	Fabrication of ASIC in MPW mode		✓
7.	Wafer Dicing, Picking and placing visually good dies in Gel Packs (40 numbers)		✓
8.	10 numbers of Packaged devices.		✓
9.	Delivery of SAC GRWS ASIC as per details in section -3		✓

Note -1: Foundry should provide latest update of Process Design Kit (PDK), which should include/support the following:

a) Mixed signal design libraries compatible with Synopsys and Cadence tools.
b) Linear & Non-Linear Scalable Mixed Signal Design models for all active and passive devices for all PVT corners including statistical and noise models.
c) Standard Digital and Analog IO pad libraries.
d) Substrate and metal definition for EM simulation.
e) ESD design library and support for the models required for the design simulation with ESD Pads.
f) Calibre and Assura compatible DRC, LVS, PEX, dummy fill files
g) Support for memory cuts of various sizes for DPRAM/SPRAM and ROM (Approx. size - 16Kx32 bit)

3 **Delivery Schedules**

Time schedule for the execution of contract shall be as per Table -2 for GRWS ASIC.

Table-2

Sr. No.	Activity	Activity Carried by	Activity duration
1	Supply of PDK and online PDK related training	Foundry/vendor	Within two months from placement of P.O.
2	DRC cleared GDSII data of GRWS ASIC submission to foundry.	SAC	-
3	DRC checks by the foundry and acceptance of GDS-II for fabrication of GRWS ASIC.	Foundry/vendor	T_0
4	Delivery of 40 number of PCM cleared visually good dies and 10 number of Packaged devices of GRWS ASIC.	Foundry/vendor	$T_1 = T_0 +$ 12months

Note:

- SAC will load GDS-II of GRWS ASIC within 24 months of PO placement.

4 **Deliverables:**

Following are the list of deliverables for GRWS ASIC:

1. 40 dies of 'GRWS ASIC' of Multi Project Wafer run of suitable 65nm/ 55nm CMOS process.
2. 10 numbers of packaged devices in compatible standard quad flat package, with in cavity size fitting to the die size.
3. Data pack consisting of: Standard PCM data including parameters given below.

S. No	Parameters
1.	Threshold voltages
2.	Breakdown voltages
3.	Saturation currents
4.	Contact resistance for vias
5.	Sheet resistance for metal layers and resistors

5 **Packaging, Storage and Transportation:**

a. Standard Quad Flat Package compatible with die size.
b. Vendor has to provide the high resolution photograph of wire bonds and pads taken before closing the lid of packages and an X-Ray of packaged devices.
c. Fabricated devices shall be packaged in ESD safe gel packs, to ensure that they are isolated from electrical, mechanical and environmental damage.
d. The packages for the devices shall be purged with nitrogen or evacuated, so that the devices are not exposed to external environment.
e. The packaging shall be so as to prevent effect of mechanical shocks, humidity and dust.

	f. In addition to other mandatory shipping marking, fragile, static sensitive warning shall be present on the shipping package.		
6	**Proprietary Rights:** The GRWS ASIC design files and fabricated chip will be under complete ownership of SAC and cannot be copied/reproduced anywhere without permission. GDS-II file shall be handed over only after signing of Non-Disclosure agreement (NDA) with Vendor and foundry.		
7	**Warranty:** 1. The supplier should warrant that the products to be supplied under this order are PCM cleared visually good dies in all respects including material workmanship, performance and shall continue to so during warranty period specified below. 2. If any defect related to fabrication is discovered or found to have developed under proper use arising from faulty materials for a period of 6 months from the date of delivery of products, then the supplier shall remedy such defects at their own cost.		
8	**General Guidelines:** a. The vendor is requested to acknowledge the receipt of this RFP and willingness/ability to respond and quote against this RFP. b. The vendor must be the authorized agency/partner/distributor of the foundry and letter of authorization/partnership should be submitted along with the quotation. c. The vendor is requested to examine the RFP thoroughly and offer point-by-point compliance/non-compliance with value. Also, mention the document name and page no in the remarks section of the RFP. The documents should be provided along with the compliance/non-compliance. d. The quotation shall consist of two parts: • PART-1: "Detailed Technical Proposal" giving all details as per RFP including commercial details with price masked. • PART-2: "Commercial Details" giving cost, payment terms and other financial details separately. e. Vendor should hold the quoted prices for the entire duration of the RFP mentioned in Table-2. f. Any rejection of die due to process relate defects has to be refabricated and delivered to SAC free of cost and delay due to re-fabrication has to be added to time schedule (Sr.No. 4 of table 2) and LD clause will be applicable. g. SAC personnel need to interact with foundry for design kit and design manual.		
9	**Line Items:** The commercial quotation should include details shown in Table -3.		

Table -3

Sr. No.	Item	Cost*
1.	Fabrication of PCM cleared Visually good dies of GRWS ASIC using MPW mode (Die size of 25 sq.mm) (Quantity: minimum 50 nos.)	
2.	Additional cost per sq. mm. of die area above 25 sq.mm. (Quantity: minimum 50 nos.)	
3.	256-pin QFP packaged devices of GRWS ASIC. (Quantity: 10 dies to be packaged out of 50 PCM cleared dies)	
Total Cost		

*** Technical Proposal should not include the cost. Cost should be masked at the time of submission of technical compliance by vendor.**

a. ***Criteria for L1 evaluation will be based on total cost of sr. no. 1 to 3 in table-3 for die size of 49 sq. mm***. However, final die size may vary depending on the design size (no less than 25 sq. mm.).
   - *Formula for total cost calculation for deciding L1:*

Total cost for L1 criteria = (S.No.1) + (S.No.2)*(24)+ (S.No.3)

b. Sr. no. 2 is optional and will be applicable only if final die size is greater than 25 sq. mm. For sr. no. 2, final cost will be considered based on the final die size at the time of GDS II loading. Payment will be released as per actual die size.
