SAC/EOSDIG/SFSD/

Request for Proposal

For

"Fabrication of CCD Controller ROIC ASIC in High Voltage CMOS process

SPACE APPLICATIONS CENTRE
INDIAN SPACE RESEARCH ORGANISATION
DEPARTMENT OF SPACE
GOVERNMENT OF INDIA
AHMEDABAD 380015

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Date: 09-10-2023

Contents

Section – 1

Introduction

Space Applications Centre (SAC) is a significant research and development Centre of the Indian Space Research Organization (ISRO). It plays a crucial role in realizing the vision and missions of ISRO. The core competence of the Centre lies in the development of space-borne and air-borne instruments/payloads and their applications for national development and societal benefits.

Proposer is the Agency/Organization that will take complete responsibility for this contract and will have partners for carrying out back-end design, design consultancy, foundry-specific fabrication, advanced packaging, filter manufacturing, screening and qualification, and electro-optical tests.

SAC wishes to develop an ROIC ASIC for stacked CCD/CMOS Image Sensor. Proposals are invited from Proposers having experience in manufacturing Mixed Signal ASIC / Image Sensor ROIC.

Proposer is requested to submit their technical and commercial offers separately. A Blank Commercial (commercial bid masked) bid shall be attached along with the Technical offer. Proposer shall provide cost break-up, including NRE (if any)**,** training, fabrication, testing charges, I.P. blocks, etc.
This document includes the scope of work, fabrication requirements from the foundry, wafer/chip acceptance definition, delivery schedule and responsibilities.

SAC will carry out the front-end design of the sensor with support from the proposer in the form of Design reviews, consultancy & and I.P. blocks.
The proposer will carry out the back-end design, tape out, fabrication, packaging and testing of the devices before delivery to SAC. SAC will review the Layout and provide clearance for fabrication.

The functional Performance of the Chip will be the responsibility of SAC.

It is very important for the evaluation of the offer that the proposal includes sufficient technical data on form, fit and function. The proposal submitted in response shall conform with the requirements in subsequent sections of this document. It shall also include the previous experience of the foundries and/ or authorized representatives (carrying out similar work) and the facilities available for design, fabrication and testing to meet the requirements. If this technical data is not provided along with the offer, SAC reserves the right to reject the proposal.

After the contract is awarded, any modification (if required) will be done per the contract's terms. The proposer may propose alternate tests/conditions and provide detailed analysis in case of any deviation from the requirements. In case of any deviation, the same shall be reported to SAC, and SAC reserves the right to accept or reject it.

Outline of Scope of Work

The following activities are planned to be carried out by the proposer in this contract.

1. Supply of PDK's & I.P. Blocks
2. Front End Design Consultancy, Back End Layout Design Services
3. Fabrication of die via two iterations.
4. COB packaging of the Die

Iterations

a) Two Fabrication run will be done in this project.
b) The First run will be of smaller size and will consists of Single Devices of each type viz. Single Clock driver, Single AFE, etc. (Maximum Die Size: 25 mm Sq.)
c) The second run will consist of complete chip with full functionality and will be of bigger size. (Die Size: 450-625 mm Sq.)

Responsibility of SAC and Proposer:

SAC will carry out the sensor front-end design of the ROIC ASIC. The proposer will provide design consultancy, IP Blocks and reviews and carry out back-end layout designs. The proposer will fabricate the ROIC ASIC, followed by packaging in COB. The functional Performance of the Chip will be the responsibility of SAC.

Right to Participation:

SAC / ISRO personnel shall participate in/ monitor any tests and inspections covered in this document. The supplier shall submit a schedule of activities, including the significant milestones. If any test/qualification is to be carried out at a place other than the manufacturer's, the supplier shall make appropriate arrangements for the participation of SAC / ISRO personnel(s).

Section – 2

Proposer Capabilities & Selection Criteria

Process Capabilities

The offered process shall meet the following requirements as a minimum.

Fabrication Process:

1. BCD Process on Si/ SOI with support for Negative Voltage Islands.
2. High Voltage >30 V & small transistors, Low VT, Low noise MOS (1.8 V/3.3 V) in the same Process
3. CMOS Technology: 0.09/0.11/0.13/um with 2/3 Metal Gates or more
4. Process shall support MLM (Multi-layer masks) to realize bigger die's

Chip Package Details

1. Maximum Area of the chip shall be in between 450 to 625 mm Sq.
2. Maximum Number of IO in the chip are less than 200 Pins
3. The Package shall provide PGA (Pin Grid array) type of Pin arrangements
4. The Type of IO's are Analog , Digital CMOS, LVDS , High Voltage Clocks , High Voltage Power rail.

Packaging Facility Capabilities

1. COB / COTS package with pin grid array frame design and fabrication
2. Die attach process with maintaining planarity.
3. Wire bonding capabilities: Aluminium/ Ribbon/ Gold Ball with a diameter of less than 1 mils

Vendor Compliance, along with the proposal

Proposer shall necessarily submit along with the proposal compliance to the process offered, Capabilities for Back End Design, Design consultancy, etc. as per the requirements of this document. In absence of these details SAC can reject the offer.

Section – 3

Realization Plan, Responsibilities & Detailed Work Package

Realization Plan

The work involves the development of an integrated image sensor. Responsibility sharing is as follows:

SAC Responsibilities

1. SAC will carry out the front end design of the ROIC
2. SAC will also carry out design reviews for layout and packaging

Proposer's Responsibility

1. Support in the form of design reviews, consultancy, and supply of I.P. blocks.
2. Carry out the back-end design, tape out, fabrication, and packaging of the devices before delivery to SAC.
3. Proposer shall develop the chip layout and mask sets based on the design submitted by SAC and fabricate these chips in a High Voltage process.
4. Proposer shall impart sufficient foundry material for designing the circuits on Cadence software and shall supply soft & and hard copies of the foundry manual and also provide suitable PDK, standard cell library and I.P. blocks to SAC at the start of each iteration. Foundry shall also offer the Cadence-compatible Design Rule Check file.
5. Proposer shall include Process Control Monitors (PCMs) on each Wafer during fabrication. D.C. parameter testing shall be performed on the PCM. The PCM set for monitoring process parameters shall include implant levels, transistor characteristics, polysilicon resistivity, and channel potentials at a minimum.

Design Reviews

Preliminary Design Review
During this step, circuit layout will be reviewed and approved jointly by the Proposer and SAC.
Critical Design Review& and tape out
The deep and exhaustive design review will include topics regarding design specifications, process spread, sensitivity, yield analysis, stability, voltage and current handling, parasitic coupling effects, chip environment simulation, temperature effect, simulated architecture, layout library conformity, Tile Layout, DRC & MASK, On wafer measurement, Dicing/visual inspection/picking and off-chip component effect shall be discussed during design reviews.

Section – 4

Requirements from the Proposer during the Kick-off Phase

<table>
<tr><td>1.</td><td>Process Development Kit (PDK): Foundry-specific PDK will establish a link between the SAC design and fabrication at the foundry. Foundry shall provide Cadence toolchain-supported analog and mixed-signal PDK, which shall consist of schematic symbols, technology files, parameterized cells (PCELLs) for custom layout realization, technology files for design rule check (DRC) and methodology to establish a channel between the DRC/LVS/ LPE (Layout parasitic extraction) rule deck. The PDK shall have silicon-qualified digital, analog, and electro-optical library elements, complete sets of low-voltage devices (1.8V and 3.3V) with various gate oxide thicknesses, and high-voltage devices up to 40V in the same process.</td></tr>
<tr><td>2.</td><td>Table 4.1 shows identified tool sets in the Cadence environment for various steps, from schematic design to layout and for the GDS-II generator, along with supported simulation tools for design verification at each stage. The proposer shall confirm PDK compatibility against that.</td></tr>
<tr><td>3.</td><td>Table-4.1: Identified toolset for foundry PDK compatibility</td></tr>
<tr><td>4.</td><td>
<table>
<tr><th>Application</th><th>Cadence Tool</th></tr>
<tr><td>Schematic design</td><td rowspan="5">Cadence toolset: Latest Version with Mentor/ Siemens tool for verification</td></tr>
<tr><td>Simulation
(verification and post layout)</td></tr>
<tr><td>Physical Block Layout and chip assembly</td></tr>
<tr><td>Physical Verification (DRC, LVS, LPE)</td></tr>
<tr><td>Layer Stream out (GDS-II generator)</td></tr>
</table>
</td></tr>
<tr><td>5.</td><td>In case the Proposer uses different tool set , then the proposer shall ensure tool compatibility with SAC version.</td></tr>
<tr><td>6.</td><td>Standard Cell Library Components: Foundry shall provide standard library components required for analog and digital block developments for SAC engineers. Offered standard cells shall have capabilities to meet the overall design goals. The foundry shall provide detailed electrical characteristics of each of the standard components at the time of submission of the technical proposal. Table 4.2 shows the minimum standard analog cells required and their electrical characteristics.</td></tr>
</table>

7.

Table 4.2: Standard analog cells required along with electrical characteristics parameters

Sr No.	Standard Cell	Purpose
1	1.8V NMOS & PMOS	Digital high speed
2	3.3V/5V NMOS & PMOS	Analog blocks
3	3.3V/5V Bipolar devices	Analog blocks
4	30/40 V Transistors	Analog Clock driver blocks
5	Poly and metal resistors	Analog & Digital
6	Contact and via resistors	Analog and digital
7	Metal-insulator-metal capacitors	Analog and digital

8. Apart from these, the foundry shall also provide standard digital cells for developing a digital section of imaging sensor. Table 4.3 shows tentative standard digital cells that the foundry shall provide as a part of the standard cell library.

9.

Table 4.3: Standard digital cells required as part of the library

Standard Cell	Parameters shall submitted by the foundry
Inverting and non-inverting buffers	Drive strength, Height and width, rise/fall time, setup and hold time requirements, load capacitance, power dissipation
2/3/4-input AND, OR, NAND, NOR, XOR, XNOR gates	
Inv& Non-Inv tri-state buffers	
Flip Flop, Latches	

	I.P. Blocks
10.	Proposer shall provide a Full Schematic Layout Design (DRC cleared) for the offered I.P. Blocks.

11.	The proposer shall ensure comprehensive documentation on the PDKs covering the detailed design document.
12.	Proposer shall assign I.P. usage rights to SAC for all future projects.
13.	Proposer shall provide comprehensive step-by-step training on designing and using the I.P. Blocks to SAC.
	The proposer Shall provide the I.P. blocks of , LVDS Drivers, PLL, and SPI block and all other blocks defined during the kick off phase.
14.	Proposer shall introduce to the foundry to get an NDA, thereby enabling the SAC to get access to the PDK. And then proposer can to set up the PDK's in SAC

Section – 5

Requirements from the Proposer during the Design Phase

	Design Phase Requirements
14.	During the design iteration, the proposer shall provide design consultancy to SAC engineers through dedicated support through Proposers.
15.	The proposer should assist in providing technical support to the SAC engineers within 24 hours.
16.	Debugging issues and problems at the Die level
17.	Proposer should participate in the Preliminary Design Review (PDR), Critical Design Review (CDR) and Final Results Review (FRR) and should provide critical feedback to make the design functional.
18.	The proposer shall Guide SAC Engineers in achieving the desired performance.
19.	The Scope of design Consultancy is during the entire iteration, typically running for 12 months from project kick-off. The estimated time of design consultancy during each iteration is 500 hours.
20.	Proposer shall visit SAC/ISRO during the Project Kick-off meeting and design reviews (desirable). The rest of the design consultancy shall be achieved through conference calls, emails or WebEx. The rest will be achieved through conference calls, personal meetings, emails or WebEx.
21.	Proposer should also help SAC engineers in Debugging potential design error issues of non-functional devices during testing and characterization iterations at SAC.
	Front End Design Consultancy
22.	Proposers will conduct regular Design reviews of the Analog / Digital designs done by the SAC.
23.	Proposer should provide the Consultants' details and share their experience in developing or guiding CMOS / CCD Sensors or Mixed Signal ASIC's. These details are necessary to ensure compliance. Proposer shall have prior experience (2-5 years) in Front end design of Mixed signal ASIC's.

	Back End Design & Tape out
24.	The proposer will do all Back-end Design for the CMOS ASIC (Layout, LVS, DRC). Front-end Design simulations will be done by SAC. The proposer shall carry out the necessary Post Layout simulation using SAC supplied test bench/ test vectors after carrying out Parasitic extraction and Update the schematic to match the performance required by the SAC.
25.	Back End Design effort shall also include parasitic extraction minimization of the parasitics to meet the Sensor and I.P. requirements. Any re-simulations based on the extracted circuits shall be carried out iteratively by the proposer. Proposer should carry out Static Timing Analysis (STA) and timing closure on final design.
26.	Insertion of I.O. Pad library for each pin. Pin planning (in consultation with SAC) will be done by Foundry Proposer in consultation with SAC.
27.	The proposer will incorporate necessary DFM guidelines to enhance the yield of the chip layout, like Metal filling, etc.
28.	The proposer will carry out a comprehensive yield assessment based on the layout and provide Yield values to SAC before taping out.
29.	The proposer Shall also provide all the layout files to SAC with documentation.
30.	Design Trade-off: The critical characteristics of the circuit should be discussed for each design. A clear trade-off should be performed, including, as a minimum: The effect of the trade-off should be reported on Electrical performance Sensitivity to temperature & and supply voltage variations Process Variation Assembly, integration and packaging
31.	All the final GDS files including modified Front end design files in a hierarchical manner design layout shall be shared with SAC with proper documentation.
32.	The layout design and the calculated yield are the responsibility of the foundry. If the anticipated yield is low, the vendor shall increase the wafer lot appropriately so that the deliverables to SAC are met.
	Package Design

33.	COB Package / PGA Package will be designed and fabricated by the proposer
34.	Proposer shall carry out Signal Integrity simulations on the package design Files and submit them to SAC for Design review and approval.
	Design for Test (Desirable)
35.	Proposer shall Design additional circuits (over and above the SAC-designed circuits) to enable ATPG (Automatic Test Pattern generation) based on Open and short detection during D.C. tests. Proposer should insert scan-chain and other DFT related test structures to achieve at least 95% test coverage. (Desirable)
36.	The circuits are preferred to be based on standard JTAG chains / etc.
37.	The proposer shall ensure the performance of the ROIC circuit is not degraded by adding such circuits.
38.	The proposer shall also share the detailed circuit designs for such an effort with the SAC team.

Section – 6

Packaging & IP Block Requirements

	Introduction:
39.	The Chip on board package must provide an electrical interface with a sensor die, mechanical support to the sensor die and environmental protection.
40.	The Packaging activity consists of the following activities:
41.	Package Mechanical Design or Usage of COTS Package
42.	Multi-Layer Electrical Design of the COB layers or Usage of COTS Package
43.	Fabrication of the Bare Package
44.	Assembly of the Die inside Package, including thermal layer implementation
45.	Wire Bonding Between Package & Die
46.	**Mounting interface:** The package shall have provisions (minimum of three mounting holes with diameter ≥ 3.2mm) to enable adequate mechanical mounting. The mounting mechanism of the sensor shall be such that proper support is provided to withstand the mechanical stress during satellite transport, launch and deployment, ensuring reliable operation throughout its life. Mounting configuration shall be proposed by the proposer and shall be mutually agreed upon. It is desirable that the mounting surface shall have flatness better than ±5µm for stress-free assembly.
47.	**Package dimension:** Dimensional details of the sensor package shall be provided by the proposer in the form of engineering drawings.
48.	**Package material and electrical interface:** The package is preferred with a Pin grid array / LGA / BGA configuration for electrical contact pins. Proposers can also provide an option for passive components to be mounted inside the package.

Sr No	IP Block	Specifications
1	LVDS Driver & receiver	• Driver Differential steady-state output Voltage: 350±50 mV at Load Resistance of 100 Ohm • Driver Offset Voltage: 1.125 to 1.375 V • Transition Time: 1ns • Driver Output Rate: up to 50 MHz • Receiver input threshold voltage: ± 100mV • Propagation delay < 2 ns • Up to 400 Mbps Switching rate
2	SPI Block	• Four Wire SPI Interface, MOSI & MISO modes • Configurable SPI Data width (8,16,24,32 bits wide) • Shall support Tx & Rx FIFO with configurable Depth

		• Data rate: 20 MHz
3	PLL Frequency Generator	• Reference Frequency: 10 MHz • Output Frequency Range: 1 MHz to 1000 MHz • Jitter ≤ ± 1 ns • Lock time ≤ 5ms

Section – 7

Test Setup

Proposer shall provide a Test Setup to carry out the testing of this chip with the actual CCD. SAC will provide the interface document for the CCD with all the electrical interfaces and the driving condition.

The test Setup shall permit following features:

- Shall provide a Socket Based CCD Front end electronics board
- Shall provide a Bias & Clock driver interface to the CCD through the developed ASIC
- Developed ASIC shall be mounted on a socket to permit testing of all the ASIC's sequentially
- The electronics boards shall be submitted to SAC for approval before its fabrication
- A PC Based Digital Data acquisition system shall be provided to control the CCD ROIC ASIC and acquire the data to PC for analysis and testing for CCD Video rates of 5 MHz or more for all the 16 channels.
- A python software shall enable the analysis of CCD data and computing of electro-optical performances of the sensor (Linearity, PRNU, DSNU, VCTI, HCTI, FWC, PTC)
- The Setup shall provide all necessary Opto-electronic hardware for carrying out the optical test of the CCD in this test conditions. Proposer shall provide the details of the test hardware proposed , so that all the electro-optical tests mentioned above can be demonstrated with the developed ASIC and the CCD.

Section – 8

Deliverables & Time Line

49.List of the deliverables to the SAC:

Sr. No.	Deliverable	Item	Qty	Payment Milestones
1.		PDKs & I.P. Delivery	One lot	
2.		PDR: Front End Design Reviews, Consultancy, Support Services	1 Lot	
3.		CDR: Sensor Back End Layout Design	1 Lot	
4.		Run-1 ROIC ASIC COB Packaged	10	
5.		Run-2 ROIC ASIC COB Packaged	40	
6.		Test Setup	1 Set	

DELIVERY SCHEDULE

The schedule shall be as per the table below.

Sr no	Activities	Timeline
1	Kick Off meeting	T0
2	Delivery of PDK & I.P. Blocks	T1= T0 + 3 months
3	Front End ROIC Design Completion by SAC including Reviews	T2
4	Run-1 COB ROIC ASIC Delivery By Proposer	T3 = T2 + 9 months
5	Front End ROIC Design Completion by SAC including Reviews	T4
6	Run-2 COB ROIC ASIC Delivery By Proposer	T5 = T4 + 9 months
7	Test Electronics	T5

Section – 9

Acceptance Criteria

	ACCEPTANCE CRITERIA
	This section covers SAC acceptance criteria for deliverables.
50.	**PDK, I.P. Cores, Back End Layout Design**
51.	Verification of the PDK & I.P. elements in the Cadence / Mentor tool by SAC
52.	IP Elements re-simulation by SAC and performance meeting based on the I.P. specifications in simulations
53.	Back End Layout Design: Based on the DRC, LVS and Parasitic extractions checks at SAC and meeting the subsequent requirements defined during Kick-off and RFP chip specifications.
	Die of the Sensor
54.	Performance of PCM within the specified limits.
	Packaged Device
55.	Performance of PCM within the specified limits.
56.	Electrical Performance of the I.P. Blocks in D.C. & lab Environmental tests
57.	Chip Specifications as defined in the Kick off phase.
	Test Electronics
58.	Capabilities to Provide a Test board with Socket based CCD Interfacing to Socket Based developed ASIC
59.	Data Acquisition system to acquire the CCD Video at rates up to 5 MHz to PC for analysis & Demonstration of CCD Electro-optical performance measurement using this developed ASIC.
	Warranty

60.	Proposer shall define storage conditions (Temperature, humidity, pressure, Atmosphere) to meet a storage Life of 5 years. The deliverables should be warranted for 1 year from the date of delivery.

Annexure A: Commercial Requirements

- Proposer are requested to submit their technical and commercial offers separately in sealed covers. Blank Commercial (price masked) bid shall be attached along with the Technical offer.

- Proposer Shall provide a detailed Cost Break up for the programme with clear bifurcation in cost for Chip fabrication, design consultancy, training, IP Blocks & testing.
- Format for quotation shall include the following costs bifurcation: (Only in the Price bid). No price shall be provided in the technical bid)

Sr no	**Item**	**Costs**
1	Engineering Cost (PDK , IP, Design consultancy , Reviews, Back end design , tape out)	
2	Iteration -1	
3	Iteration-2	
4	Dicing & Packaging	
5	Test Electronics	
	Total	

- Proposer shall provide clear milestones for payment delivery as per the suggested table in the deliverables section.

- SAC can decide to close the PO after iteration-1 in case the performance from the run-1 have multiple issues

Annexure B: Chip Design Technical Specifications

CCD Clock Type	Number of clocks per band	Total number of clocks for 6 bands	Load	High Level	Low Level	Amplitude	Typical Rise/fall time	Peak Current(A)
Vertical Register	4	24	8.5 nF	+2 to + 13	-9 to +2	9 to 13	40 ns	2.7 A
Stage Selection	6	24	200 pF	+2 to + 13	-9 to +2	9 to 13	40 ns	65 mA
Transfer Gate	3	18	200 pF	+2 to + 13	-12 to +2	10 to 18	40 ns	90 mA
Horizontal Register	4	24	300 pF	3 to 13	-10 to + 2	6 to 13	10 ns	390 mA
Last Gate	8 (Can be combined in 1 clock)	48/6	100 pF	3 to 13	-10 to + 2	6 to 13	5 ns	260 mA per clock = 2A per 8 clocks
Reset	8 (Can be combined in 1 clock)	48/6	50 pF	7 to 13	0 to 4	8 to 15	2 ns	375 mA per clock = 3A per 8 Clocks
Total clocks	33/19	102						
Band Independency removed		67						

- Programmable Rise / Fall time
- Tristate Feature for the clocks
- Tristate to Fixed potential for stage selection clocks

Feature	Range	Performance	Resolution	No. of channels	Load
Bias Generation	0 - 20 V	Noise < 1 mV	Step Size = 0.1 V	32	Current Per channel = 20 mA
Clock Generation	Line Rate Up to 40 KHz Readout Rate up to 15 MHz	Jitter < 100 ps	Step Size = 1ns	150	Clock Driver
Clock Driver	Programmable High Low / Rise Fall	Amplitude up to 20 V Rise fall up to 1 ns	0.1 V & 1 ns Delay	150	Up to 5nF
Video Processing Buffer Ampl + CDS + AFE	2 V Signal of CCD Unbuffered	1 bit System Noise < 10e-	16 bit	24-96	Rate up to 15 MHz