Development of Drive Electronic Hardware for Interline CCD Imager

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1. Introduction

Sensor Development Area (SEDA) is involved in design and realization of electro-optical payload for remote sensing applications. Charge Coupled Devices (CCD) are utilized as a sensing element for realization of E-O imaging payloads. These devices are required to be tested and characterized thoroughly prior to their use for payload realization.

In order to characterize CCDs, the drive electronics and acquisition hardware are employed. Drive electronics hardware generates necessary high voltage clocks and low noise biases for CCD operation. In addition, acquisition hardware performs signal conditioning, digitization, storage, acquisition and display of CCD pixel data. CCD drive & acquisition hardware together forms CCD characterization test-bench along with associated test instruments.

As part of this development, CCD drive electronics and acquisition hardware is to be developed.

CCD drive electronics & acquisition hardware needs to be realized within a fixed form factor of 16200 mm^2 /PCB, with the complete functionality divided in up to four PCBs. (Two PCB option is preferred). Exact sizes of PCBs are to be decided at the time PCB design phase after PO placement.
This H/w should be realized using industrial grade components. Vendor has to carry out necessary burn-In tests on realized hardware.

Following are the activities to be carried out be vendor for realization of CCD drive electronics & acquisition hardware.

1. schematic & PCB layout design
2. Bare PCB fabrication
3. Component selection & procurement
4. Soldering and assembly of components
5. Firmware development for FPGA / microprocessor
6. Test hardware and software development for thorough testing of design including digital data acquisition, commanding etc.

Following are the SAC responsibilities

1. Provide detailed specification of hardware to be developed
2. To review design at each stage and approve for next stage
3. Component selection review and approval
4. Providing any other document required by vendor as per agreement
5. Any other documents, reviews as agreed upon

Techno-commercial proposals are invited from reputed vendors having at least 2 years' experience in development of mixed signal drive H/w design, development and testing. This document gives test h/w details, vendor scope of work, components list, delivery schedule and deliverables in the subsequent section.

Vendor Selection Criteria:

1. Past experience of at least 3 years in mixed signal electronics h/w design
2. Detailed execution plan for development explaining how proposed H/w would meet the CCD datasheet goals & size constraints
3. Design goal (specification) achieved from past similar type of H/W
4.. Designers background and their experience (design team must have more than 3 years of relevant experience)
5. Reference from the previous consumer (minimum one reference is required)

This document gives details of the development in the following sections:
Section-1: Introduction
Section-2: Interline CCD Drive Hardware Configuration
Section-3: Vendor Scope of Work and SAC responsibility
Section-4: Electrical Bias and Timing details
Section-5: Deliverables
Section-6: Acceptance Criteria
Section-7: Delivery Schedules
Section-8: Warranty

2. Interline CCD drive electronics & acquisition H/W

For the preferred configuration of two PCB based solution,

2.1.1 Bias and timing card consist of (a) Detector foot-print for housing interline CCD (b) FPGA for CCD timing clock generation & SPI interface for CCD clocks configuration (c) CCD clock drivers for translating FPGA signals to high voltage CCD clocks (d) Low noise CCD biases generation (including –ve biases) (e) FPGA bias regulators (f) signal conditioning & video buffer circuits within a single PCB board and (g) USB based micro-controller for Host PC interface and SPI configuration. Vendor may choose the components (FPGA, µC, clock driver and regulator) based on the no. of CCD clocks, their swing and required CCD biases meeting noise and swing requirement for CCD operation. The required CCD operating frequency (pixel readout rate) is 40 MHz.

Bias, video pre-processing and timing hardware design must ensure signal integrity of high voltage CCD clocks and appropriate shielding of CCD output (ensure ground plane bounce <250 uV (Vrms)) at 40 MHz frequency of operation.

2.1.2 Control, processing and storage card carry out the (a) correlated double sampling (CDS) (b) four-channel digitization of CCD data (c) storage of CCD frames in on-board memory and, (d) Provides USB and space wire interface for stored/acquired digital data acquisition. (e) CCD Data processing using FPGA, which generates digitization and serialization clocks, memory read/write clocks and streaming of CCD data from memory to USB & space wire Interface. Vendor has to select the on board memory size based on CCD data volume generated during 15 min imaging duration at 40 MHz operation.

Hardware control, data acquisition and post processing software is the part of CCD Drive electronics hardware. Below figures-1 shows the overall scheme for proposed hardware configuration.

Power will be provided by a raw bus supply. On-board processor command interface will be provided for streaming CCD data over space wire interface only. The interfacing among the cards can be done using flexi/FRC cables or as per vendor's preferred option considering the availability of space within the structure.

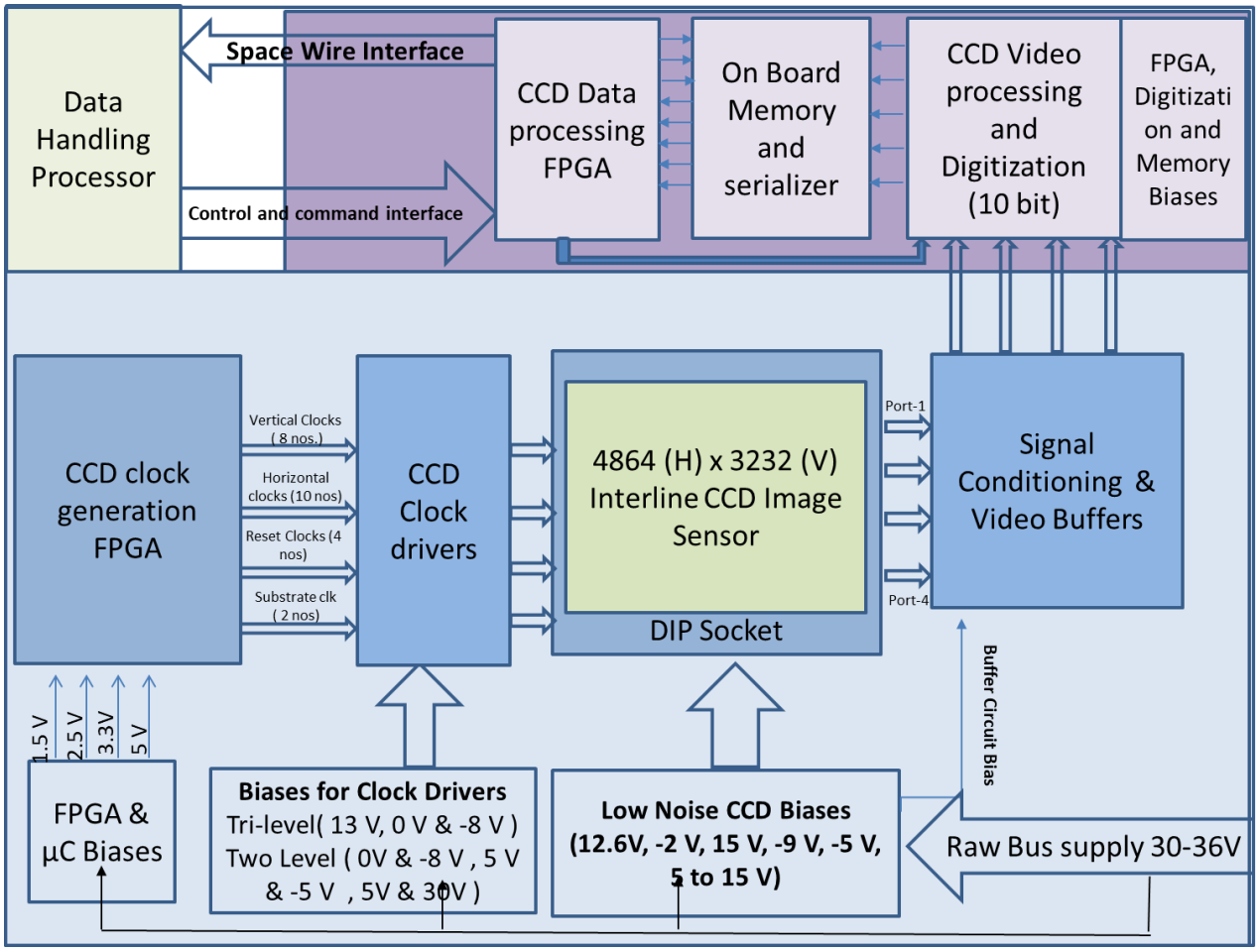


Figure-1: Interline CCD drive electronics & acquisition H/W

3. Vendor Scope of Work

3.1 Vendor Scope of Work

Major responsibility of the vendor for the development are listed below

- PCB schematic & layout from functional block diagram (as per figure-1) provided by SAC within prescribed size and specified no of cards.
- Fabricate the PCB boards and supporting hardware as per the quantity specified in the deliverables.
- Procure the components
- Carry out the assembly and testing of cards as per the requirements provided by SAC
- FPGA, Microprocessor code designs wherever applicable as per required functionlity

- Vendor requires to develop the (a) FPGA based firmware for generating CCD timing under different modes (b) FPGA based firmware for digitization control & processing, storage & streaming of CCD data and implementation of space wire and USB interface for acquisition (c) micro-controller based software for host PC USB interface, SPI interface, bias monitoring and power sequencing. (e) Post-processing software.
- Depute the design/fabrication engineer for hardware support during DUT testing for minimum of 1 and half year at SAC premises. Engineer must have been part of hardware realization team and should have working knowledge of required software development, FPGA and micro-controller firmware development.
- Arrange for test equipment (power supplies, multi-meter, oscilloscope etc) for assembly and testing of PCBs boards at his premises. For complete chain's performance evaluation and calibration, vendor has to develop dummy load card that can generate simulated video output like CCD.
- Develop the complete development and testing plan explaining each activity (like component mounting, card testing, integrated testing etc.) in details PCB and has to submit to SAC before initiating the assembly & fabrication.
- Develop the mechanical fixtures for developed hardware packages. Mechanical drawing for the fixture is to be derived by the vendor from PCB sizes. Orientation & fixture mounting mechanism shall be mutually decided post PCB design.
- Detailed documents related to design, test results & major observation during development.

4. Electrical Bias and Timing details

Vendor is expected to go through all the specifications mentioned below and discuss with SAC team to confirm correctness of understanding before starting work.

4.1 Bias Details

The DUT biases, their tolerances and current requirement are given in the table-1.

Table-1: DC Biases Requirement

Detector biases(Nos of lines)	Symbol	Bias Requirement#	DC Current / output port	Noise Requirement
Reset Drain (2)	RDα	12.4 ≤VRD≤ 12.8	10 uA	<100uV
Output Gate (2)	OGα	-2.2≤VOG ≤-1.8	10 uA	
Output Amplifier Supply (2)	VDDα	+14.5≤ VDD≤ 15.5	11.0 mA	
Substrate (1)	SUB	+5≤ VSUB ≤+15	50uA	
ESD Protection Disable (1)	ESD	-9.5 ≤VESD≤ -7.8 V	50 uA	
Ground	GND	0	−1.0 mA	
	* Separate bias lines are required for Top and bottom half of the array in hardware. ~ approx. 8 detector DC bias will be required			

Bias requirement shown are must be tune-able within the above-specified range with an accuracy of <50 mV and step size of 100mV.

$ Refer annexure-1 for detailed pin description

4.2 Timing Clock Requirement

Table-2: DUT Clock Level and Rise/fall Requirement

Clock	High level(V)	Mid-Level(V)	Low* level(V)	Frequency (MHz)	Clock Capacitance (nF)
V1B, V1T	13V (-0.2V/+1V)	0 (-0.2V/+0.2V)	-8 (-0.2V/+0.2V)		88, 86
V2B, V2T	0 (-0.2V/+0.2V)	-	-8 (-0.2V/+0.2V)		74, 75
V3B, V3T	0 (-0.2V/+0.2V)	-	-8 (-0.2V/+0.2V)		83, 84
V4B, V4T	0 (-0.2V/+0.2V)	-	-8 (-0.2V/+0.2V)		76, 73
H1S	0 (-0.2V/+0.6V)	-	-4.4 (-0.6V/+0.2V)	40	0.36
H1B	0 (-0.2V/+0.6V)	-	-4.4 (-0.6V/+0.2V)	40	0.324
H2S	0 (-0.2V/+0.6V)	-	-4.4 (-0.6V/+0.2V)	40	0.368
H2B	0 (-0.2V/+0.6V)	-	-4.4 (-0.6V/+0.2V)	40	0.293
H2SL	0 (-0.2V/+0.2V)	-	5 (-0.2V/+0.2V)	40	-
R	3.2 (-0.2V/+0.2V)	-	-3 (-0.2V/+0.2V)		-
R2ab, R2cd	4.2 (-0.2V/+0.2V)	-	-1.8 (-0.2V/+0.2V)		-
SUB	30 (-1V/+10V)		5 to 15 V		11
FDG	+5 (-0.5V/+0.5V)		-8 (-0.2V/+0.2V)		0.117+ 0.117

- All vertical clock rise/fall time must be within 7% of it pulse width
- All horizontal and reset clock rise/fall time must be within 12% of it pulse width
- Refer the interline datasheet of CCD “KAI-16070-D-Inerline CCD Datasheet.pdf” for more information
- Tentative clock inputs required for detector are ~50

4.3 Timing Details

4.3.1 Normal Interline Readout Mode:

Inter-line CCD has four major set of clocks for it operation. Vertical clocks, horizontal clocks, reset clocks and exposure control clocks. To read out a frame from sensor vertical clock run once in frame time transferring charge from pixel to shield region. Vertical clocks then run NV number of times for transferring charge row by row. Horizontal/reset clocks then transfers out NH pixels for every row transferred. Exposure control clock can be inserted after any of the NV line transfer and before horizontal clock starts. Below figures 3,5,6 and 7 describes the timing flow sequence and timing relation for each set of clocks. Figure 4 shows a specific case of timing flow for TDI readout timing.

Timing flow chart in normal operation and exposure control mode:

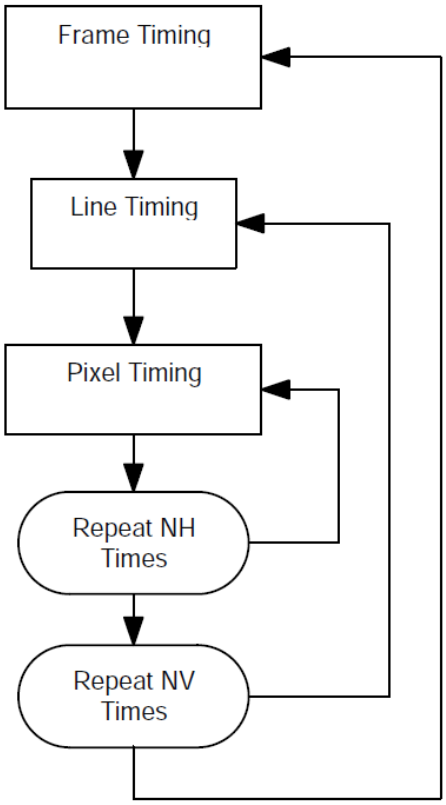


Figure-3a without exposure control

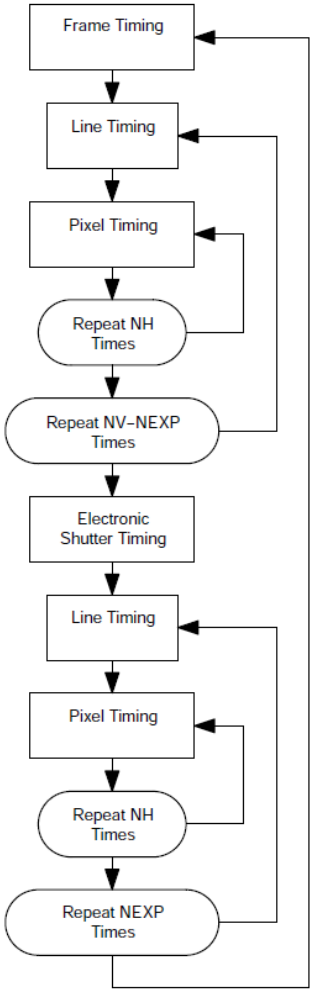


Figure-3b with exposure control

NH= the number of HCCD clock cycles per row
NV=the number of VCCD clock cycles per frame

M= the number of TDI

4.3.2 Timing flow Diagram for TDI Mode:

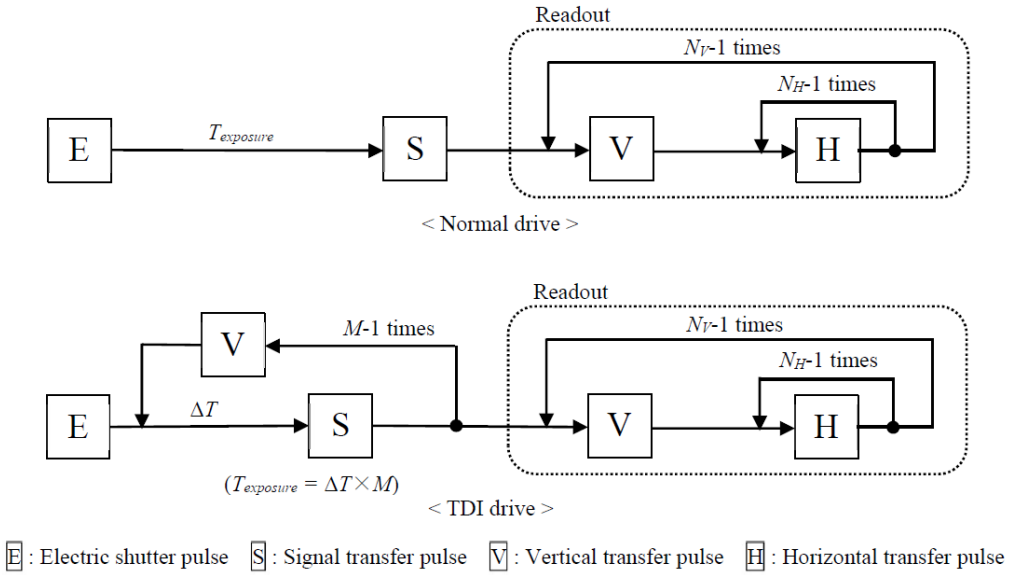
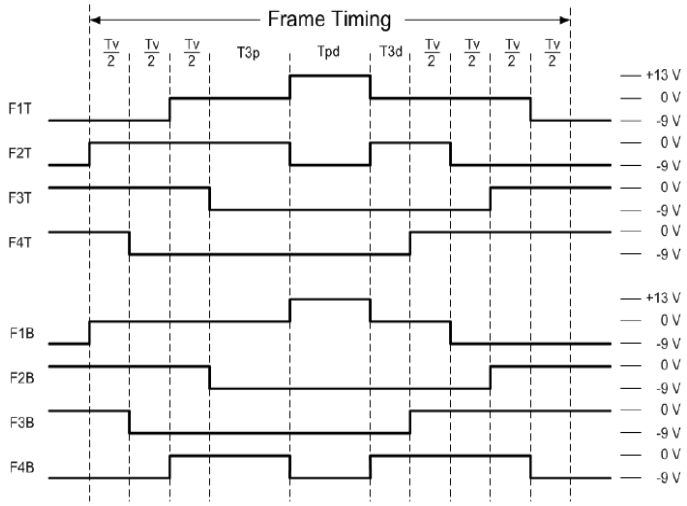
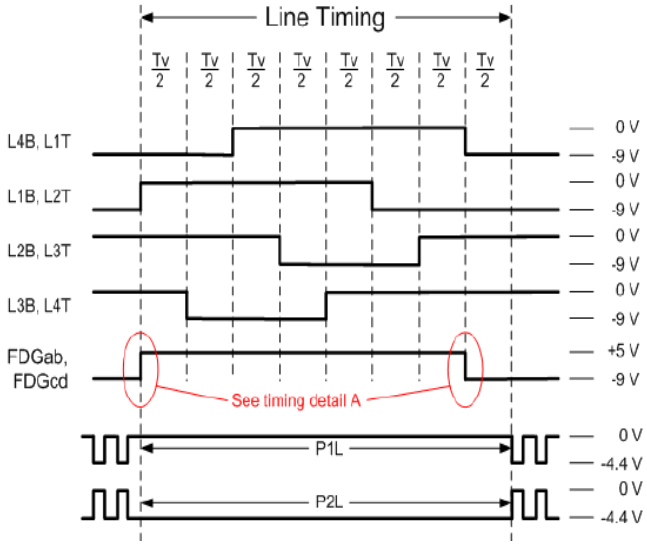


Figure-4: Interline TDI mode Read out timing flow

4.3.3 Frame Timing and Line timing (Full Resolution)



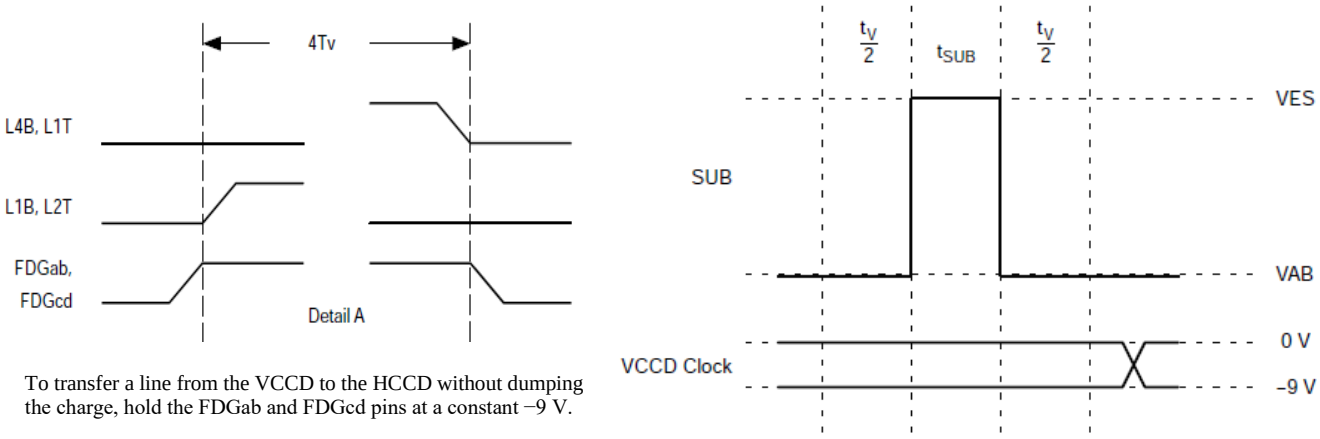
The charge in the photodiodes begins its transfer to the VCCD on the rising edge of the +13 V pulse and is completed by the falling edge of the +13 V pulse on F1T and F1B.



If the line is to be dumped then clock the FDGab and FDGcd pins as shown in detail A.

- **Tpd: 6 us (min), T3p & T3d : 16 us(min), Tv: 4 us(min)**

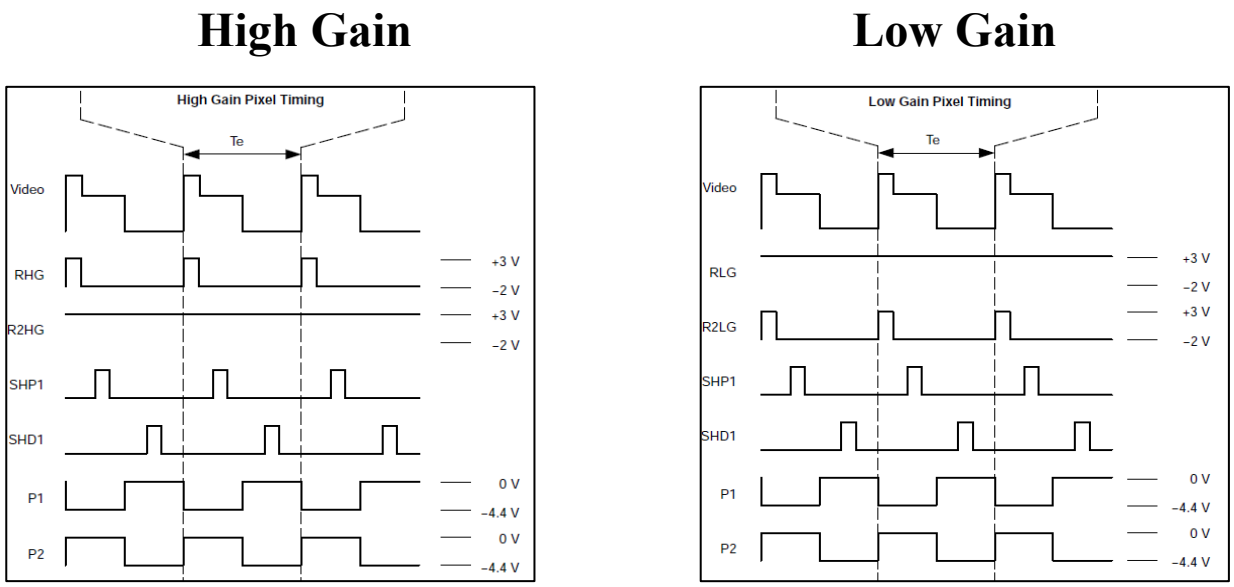
Figure-5: Frame and Line Timing Details



t_{SUB}:2 us

Figure-6: Line dump and Exposure control Timing

4.3.4 Pixel Timing Diagram



Te: 25 ns
RHG high width to be at least Te/16

Figure-7: Horizontal clock read out timing

5. Deliverables

Table-3: Deliverables

Sr.No	Deliverable	Quantity
1		
2	CCD Drive Hardware & acquisition Hardwares*	3 lot
3	Mechanical Fixtures for detector and electronics cards	2 sets
4	Layout design files for Drive hardware's	1

5	All source codes	1
6	All software	1
7	All Documents generated by vendor during course of development	1
8	Dummy loads post burn-IN of delivered H/w	1

- Based on the actual design option finalized (using 2 or 3 PCB boards design) quantity mentioned above must be delivered for each PCB board
- Testing and characterization of DUT at SAC for 3000 hours for a period of 18 months

6. Acceptance Criteria

Factory acceptance Test

- Each developed hardware should comply with the CCD bias & timing requirements as given in the section 4 electrical bias & timing requirement of this document.
- Generated biases of hardware should be variable within the limit specified in the table-1
- Clock rise/fall time and high/low level should be within the specs as given in table 2.
- All the delivered H/W required to undergo 168 hour burn-In with dummy load before delivery to SAC
- Developed H/w's will be subjected to industrial grade temperature limits.

Acceptance Test at SAC

- The developed hardware will be tested with actual load load. Performance parameters as given in the table below must be achieved in complete chain testing.
- All the delivered H/W will be subjected to repeated on-off cycles for any intermittent behavior.
- Note: Timing given in the section 4.3 of this document are reference timing and minor modification in clock relation may be required during acceptance at SAC.
- Functionality will also be verified at lower frequencies i.e <40MHz.

Sr. No.	**Parameter**	**Specification Requirement**	**Remark**
1	System rms Read Noise (mV) on CDS data with ground input	< 0.4	@ 40MHz pixel frequency, should also demonstrate the performance at 20MHz & 10MHz
2	System rms Read noise (mV) on CDS data with 20mV swing	< 0.8	@ 40MHz pixel frequency
3	Digitization bits	Minimum 10-bit	
4	On board storage	>64 GB	with 10-bit digitization

5	Exposure & Gain control	Required	To be demonstrated
7	Power	TBC (minimum)	
8	Data processing	On board data compression	

Quality Acceptance Criteria

1- All delivered PCBs must be fabricated as per ISRO PCB fabrication standard ISRO-PAX-304.
2- Vendor must maintain fabrication history record with 100% QC inspection should be deliverable to SAC.
3- Storage of materials used, partially fabricated cards, components and card testing should be carried out in controlled environment (temp.: 25 C ±3 °C and humidity: 55 to 60 RH)
4- Industrial grade quality conformance (CoC, date code etc.) should be provided for each part used.
5- Components used for the delivered hardware must be of Industrial grade or better quality.

7. Delivery Schedule

Table :10 Delivery Schedule

S. No.	Activity	Timeline
1	Fabrication, assembly and testing of Detector and Bias & Timing Cards hardware	T1=T0+8 months
2	Functional Testing and DUT screening at SAC	T2=T1+18 months

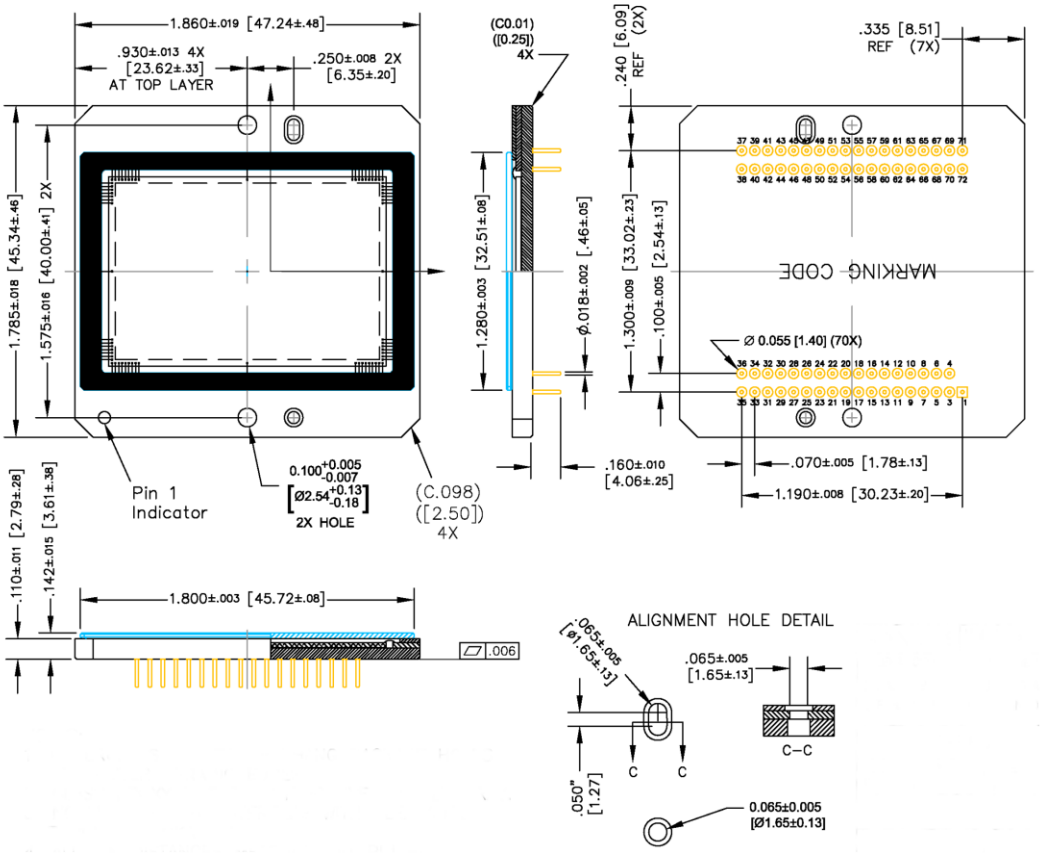
T0: PO acceptance by vendor

8. Warranty:

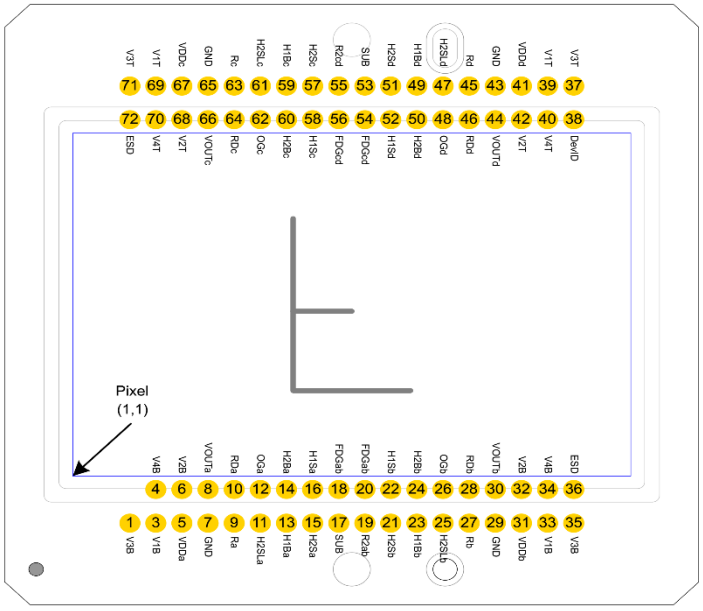
Vendor shall provide warranty for 18 months from the date of acceptance test. During warranty period, vendor shall provide support and free of cost repair of hardware's. Vendor shall provide free replacement/repair within warranty period. Vendor shall give the details of the approach to support during warranty.

Annexure -1

CCD Detector Mechanical Drawing



Pin Description and Device Orientation



Pin Description

Table 3. PIN DESCRIPTION

Pin	Name	Description
1	V3B	Vertical CCD Clock, Phase 3, Bottom
[2]		[No Pin − Keyed]
3	V1B	Vertical CCD Clock, Phase 1, Bottom
4	V4B	Vertical CCD Clock, Phase 4, Bottom
5	VDDa	Output Amplifier Supply, Quadrant a
6	V2B	Vertical CCD Clock, Phase 2, Bottom
7	GND	Ground
8	VOUTa	Video Output, Quadrant a
9	Ra	Reset Gate, Standard (High) Gain, Quadrant a
10	RDa	Reset Drain, Quadrant a
11	H2SLa	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant a
12	OGa	Output Gate, Quadrant a
13	H1Ba	Horizontal CCD Clock, Phase 1, Barrier, Quadrant a
14	H2Ba	Horizontal CCD Clock, Phase 2, Barrier, Quadrant a
15	H2Sa	Horizontal CCD Clock, Phase 2, Storage, Quadrant a
16	H1Sa	Horizontal CCD Clock, Phase 1, Storage, Quadrant a
17	SUB	Substrate
18	FDGab	Fast Line Dump Gate, Bottom
19	R2ab	Reset Gate, Low Gain, Quadrants a & b
20	FDGab	Fast Line Dump Gate, Bottom
21	H2Sb	Horizontal CCD Clock, Phase 2, Storage, Quadrant b
22	H1Sb	Horizontal CCD Clock, Phase 1, Storage, Quadrant b
23	H1Bb	Horizontal CCD Clock, Phase 1, Barrier, Quadrant b
24	H2Bb	Horizontal CCD Clock, Phase 2, Barrier, Quadrant b
25	H2SLb	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant b
26	OGb	Output Gate, Quadrant b
27	Rb	Reset Gate, Standard (High) Gain, Quadrant b
28	RDb	Reset Drain, Quadrant b
29	GND	Ground
30	VOUTb	Video Output, Quadrant b
31	VDDb	Output Amplifier Supply, Quadrant b
32	V2B	Vertical CCD Clock, Phase 2, Bottom
33	V1B	Vertical CCD Clock, Phase 1, Bottom
34	V4B	Vertical CCD Clock, Phase 4, Bottom
35	V3B	Vertical CCD Clock, Phase 3, Bottom
36	ESD	ESD Protection Disable
72	ESD	ESD Protection Disable
71	V3T	Vertical CCD Clock, Phase 3, Top
70	V4T	Vertical CCD Clock, Phase 4, Top
69	V1T	Vertical CCD Clock, Phase 1, Top
68	V2T	Vertical CCD Clock, Phase 2, Top
67	VDDc	Output Amplifier Supply, Quadrant c
66	VOUTc	Video Output, Quadrant c
65	GND	Ground
64	RDc	Reset Drain, Quadrant c
63	Rc	Reset Gate, Standard (High) Gain, Quadrant c
62	OGc	Output Gate, Quadrant c
61	H2SLc	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant c
60	H2Bc	Horizontal CCD Clock, Phase 2, Barrier, Quadrant c
59	H1Bc	Horizontal CCD Clock, Phase 1, Barrier, Quadrant c
58	H1Sc	Horizontal CCD Clock, Phase 1, Storage, Quadrant c
57	H2Sc	Horizontal CCD Clock, Phase 2, Storage, Quadrant c
56	FDGcd	Fast Line Dump Gate, Top
55	R2cd	Reset Gate, Low Gain, Quadrants c & d
54	FDGcd	Fast Line Dump Gate, Top
53	SUB	Substrate
52	H1Sd	Horizontal CCD Clock, Phase 1, Storage, Quadrant d
51	H2Sd	Horizontal CCD Clock, Phase 2, Storage, Quadrant d
50	H2Bd	Horizontal CCD Clock, Phase 2, Barrier, Quadrant d
49	H1Bd	Horizontal CCD Clock, Phase 1, Barrier, Quadrant d
48	OGd	Output Gate, Quadrant d
47	H2SLd	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant d
46	RDd	Reset Drain, Quadrant d
45	Rd	Reset Gate, Standard (High) Gain, Quadrant d
44	VOUTd	Video Output, Quadrant d
43	GND	Ground
42	V2T	Vertical CCD Clock, Phase 2, Top
41	VDDd	Output Amplifier Supply, Quadrant d
40	V4T	Vertical CCD Clock, Phase 4, Top
39	V1T	Vertical CCD Clock, Phase 1, Top
38	DevID	Device Identification
37	V3T	Vertical CCD Clock, Phase 3, Top

1. Liked named pins are internally connected and should have a common drive signal.